A MONOLITHIC 40-GHz HEMT LOW-NOISE AMPLIFIER

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ABSTRACT

A monolithic, single-stage HEMT low-noise amplifier has been developed at 40 GHz. This amplifier includes a single 0.25-μm gate-length HEMT active device with on-chip matching and biasing circuits. A gain of 6.5 dB and a noise figure of 5 dB were measured from 38 to 44 GHz. By replacing the triangular gate profile with a mushroom gate profile, the amplifier achieved 8-dB gain and 4-dB noise figure from 36 to 42 GHz. The chip size is 1.1 x 1.1 mm.

INTRODUCTION

HEMTs have demonstrated their superior gain and noise figure performance over conventional MESFETs [1]. State-of-the-art gain and noise figure performance has been achieved from monolithic amplifiers [2] using HEMTs at frequencies below 20 GHz. Above 20 GHz, reports were made on the monolithic amplifiers using both MESFETs [3-4] and HEMTs [5-6] as active devices for low-noise applications.

This paper describes a monolithic, reactively-matched 40-GHz low-noise amplifier using a 0.25-μm HEMT as the active device. The amplifier with a triangular gate profile has achieved approximately 6.5-dB gain and a 5-dB noise figure from 38 to 44 GHz. The gain of the amplifier increases to 8 dB and the noise figure decreases to 4 dB when the gate is replaced by a mushroom gate profile. This is the best reported result for a single-stage MMIC amplifier over this bandwidth.

DESIGN CONSIDERATIONS

Figure 1 shows the HEMT epitaxial growth structure used in this amplifier. These HEMT layers were grown by MBE at 580°C on GaAs,

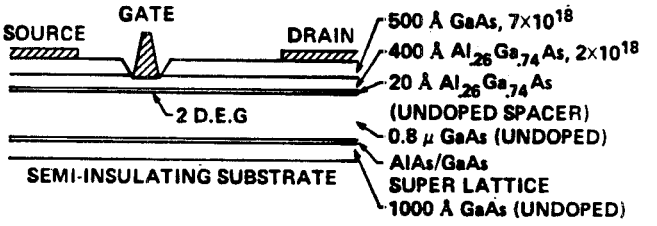

Fig. 1 Cross section of HEMT device.

which was unintentionally doped n-type at about 1 x $10^{14}/cm^3$. A five-period AlAs/GaAs superlattice was grown midway into the buffer layer in an attempt to reduce dislocations and improve surface morphology.

Figure 2 shows the equivalent circuit model for a discrete 0.25 x 150-μm gate-length HEMT with a triangular gate profile biased for minimum noise figure. The gate is π-configured, and the source-drain spacing is 2.5 μm. This HEMT has a measured minimum noise figure of

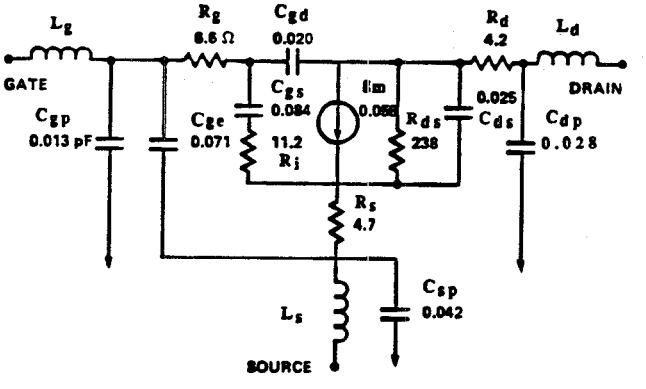

Fig. 2 Equivalent circuit model of 0.25 x 150-μm HEMT device.

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1.4 dB and associated gain of 12 dB at 18 GHz. The predicted F_{min} is 2.74 dB at 40 GHz using Fukui's expression.

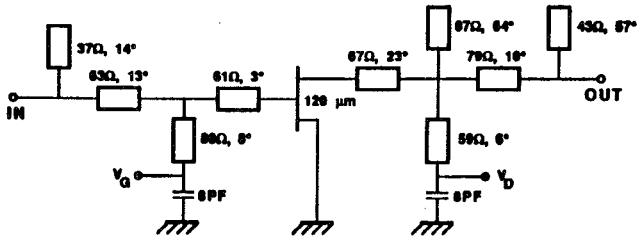

Fig. 3 Schematic circuit diagram for monolithic 40-GHz amplifier. The electrical lengths of the transmission lines are given at 40 GHz.

A 44-GHz reactively-matched amplifier was designed using the HEMT model in Fig. 2. Figure 3 shows the schematic layout of this amplifier, which uses open stubs, shunt-shorted stubs and transmission lines as the input and output matching elements. The electrical lengths of the transmission lines are given at 40 GHz. Nineteen design parameters, including the matching and biasing circuit elements along with the gate periphery, were optimized for a maximum flat gain performance from 42 to 46 GHz using SUPERCOMPACT™. The impedance of the matching elements was constrained to be within the range from 30 to 90 Ω, for the purposes of practical realization and an acceptable transmission line loss. A simulated gain of 7.5 dB from 40 to 46 GHz was obtained, as shown in Fig. 4.

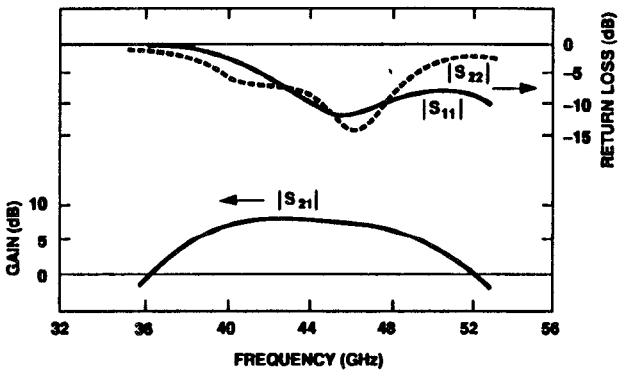

Fig. 4 Simulated gain and return loss performance of the monolithic 40-GHz amplifier.

AMPLIFIER FABRICATION

Standard processing techniques were used for most of the 40-GHz HEMT amplifier fabrication. Isolation was achieved with a 2500 Å mesa etch. The 0.25-μm gate was written with a Cambridge EBMF 10.5 E-beam machine using PMMA resist. A sputtered SiO_2 layer of 2000 Å was used as the capacitor dielectric material. In order to achieve good RF grounding, 60 x 60-μm backside vias were incorporated using reactive ion etching. All other process steps used conventional metallization, liftoff and pulse-plating techniques.

Figure 5 shows a photograph of the 40-GHz amplifier. The chip size is 1.1 x 1.1-mm, and the layout of the circuit is compatible with the Cascade Microtech RF wafer-probing technique.

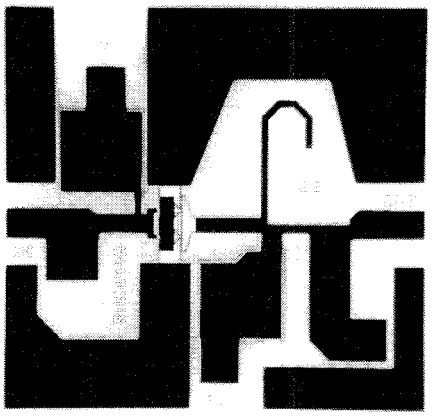

Fig. 5 Photograph of the monolithic 40-GHz amplifier. Chip size: 1.1 x 1.1 mm.

MEASURED GAIN AND NOISE FIGURE PERFORMANCE

A gain of approximately 6.5 dB from 38-44 GHz (biased at V_{ds} = 3V and I_{ds} = 15 mA) and an input/output return loss of better than 10 dB from 39-43 GHz were measured as shown in Fig. 6. Measurement was accomplished using the waveguide-based HP-8510 network analyzer with full error corrections and the 50-GHz Cascade probes. The measured peak gain agrees well with the simulated result, but the peak frequency is shifted from 44 GHz down to 41 GHz. This is probably due to the higher gate

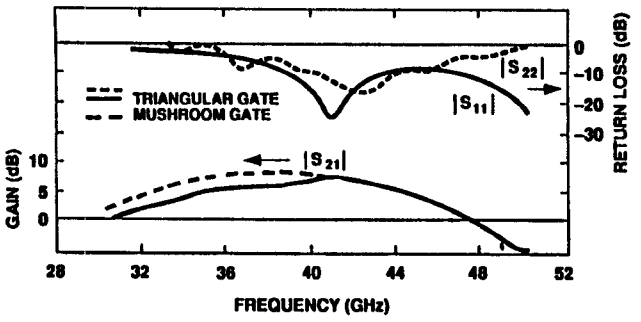

Fig. 6 Measured gain and return loss performance of the monolithic 40-GHz amplifier.

capacitance of the device than the value used in the device model.

A preliminary measurement on a recent wafer indicates higher peak gain (10 dB) and higher peak frequency (43 GHz) than the result shown in Fig. 6. The higher stable gain performance could be related to an increased amount of positive feedback due to changes in some of the device small signal parameters. The higher peak frequency is related to a lower gate capacitance of the device in the circuit. This wafer is currently under investigation.

Figure 7 shows approximately 5-dB measured noise figure for the 40-GHz amplifier from 38 to 44 GHz when biased at minimum noise bias conditions. The amplifier noise figure below 40 GHz was measured with an HP-R347B noise source and a HP noise measurement system using the waveguide test setup and the Cascade prober. Above 40 GHz, the measurement was performed using a gas tube noise source with the amplifier bonded on a finline fixture.

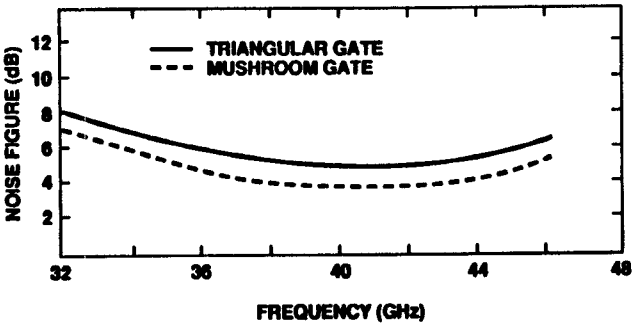

Fig. 7 Measured noise figure performance of the monolithic 40-GHz amplifier.

PERFORMANCE OF AMPLIFIER WITH MUSHROOM GATE PROFILE

The 0.25-μm gate with a mushroom gate profile has recently been developed using tri-level resist and E-beam lithography. The DC gate resistance of a 0.25-μm gate with a mushroom gate profile (70 Ω/mm) is reduced to almost 1/7 of that for a 0.25-μm gate with a triangular gate profile (470 Ω/mm). The 0.25 x 150-μm π-configured HEMT with a mushroom gate profile has a measured noise figure of 0.9 dB and an associated gain of 13 dB at 18 GHz.

A 40-GHz reactively-matched amplifier with a mushroom gate profile was fabricated on HEMT material. This amplifier gave 8-dB of gain and a 4-dB noise figure over the 36-42 GHz band (shown in Figs. 6 & 7 as dashed curves). Compared to the amplifier with a triangular gate profile, the preliminary measurement for the amplifier with the mushroom gate profile has 2-dB higher gain and 1-dB lower noise figure due to the lower R_g of the device.

MEASURED OUTPUT POWER PERFORMANCE

The 1-dB compression power was measured for the 40-GHz reactively-matched HEMT amplifier at 40 GHz. When biased at maximum power (V_{ds} = 3V, I_{ds} = 21 mA), the 1-dB compression power for the HEMT amplifier was measured to be 10 dBm at 40 GHz.

CONCLUSIONS

A monolithic low-noise reactively-matched amplifier using HEMT technology for the active device has been developed at 40 GHz with about 6.5-dB gain and approximately 5-dB noise figure from 38-44 GHz. By replacing the triangular gate profile with a mushroom gate profile, the amplifier achieved 8-dB gain and a 4-dB noise figure from 38 to 44 GHz. These are the best reported results for a MMIC amplifier over this bandwidth.

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